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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,542	09/19/2003	Thomas R. Apel	TRQ-12923	5554

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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,542	APEL, THOMAS R.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. 5,162,756 (Taniguchi) in view of Holt.

Figure 2 of Taniguchi discloses a power amplifier circuit. Note that the goal of these circuits of Taniguchi is to "obtain a high power high frequency signal" (See column 3, around line 59) and thus these circuits are power amplifier circuits. Taniguchi includes a first amplifier "subsection" FET_1 (Herein and throughout referred to just as the first amplifier.) that is configured to receive an input signal that is the unmarked signal at the node that directly connects elements L_1, L_3, and L_4. Note that the first amplifier receives this signal through element L_3. This is only giving the broadest reasonable interpretation to the claims consistent with the specification. See MPEP 904.01. The first amplifier clearly provides a "first" output signal. Element L_4 of Taniguchi is a first delay element that introduces a delay to the input signal and applies this to the input of a "second" amplifier "subsection" FET_2 (Herein and throughout referred to just as the second amplifier.). This second amplifier clearly has an output signal and provides a "first" delayed output signal to the node directly connecting elements L_3', L_4' and L_1'. The top of page 9, of applicant's specification clearly sets forth that an impedance inverter can be a quarter wavelength transmission line. Thus all the quarter wavelength lines of Taniguchi are "impedance inverters" as set forth by applicant and is in accordance with applicant's application. These impedance inverters of Taniguchi are in accordance with applicant's specification provides the "impedance inversion". Thus the impedance/delay element L_3'also introduces a second delay to the first output signal thereby creating a second delayed output signal. The node directly connecting elements L_3', L_4' and L_1' and the node directly connecting elements L_5', L_6' and L_2' in combination with the node that directly connects elements L_1' and L_2' provides the means for combining the first and second delayed output signals that ultimately provides the high frequency amplified output signal S_{out}. This output signal is provided on the output terminal "P_1' ". Taniguchi is silent on showing the bias circuit and supply circuit or what applicant calls "level control circuit" in claims like claim 1 for example that biases the first and

second amplifiers to operate in the saturation range, i.e. non-linear classes of operation. Applicant should note that while Taniguchi is silent on the bias circuit or "level control circuit". As is known to those of ordinary skill in the art, Taniguchi inherently must have a bias circuit and power supply circuit because this is a necessary circuit needed so that the amplifier(s) can operate.

The structure indicated above clearly provides for the claimed method of the claims indicated at the beginning of this rejection except for as indicated above Taniguchi is silent on providing a bias control circuit/level control circuit that biases the amplifiers such that non-linear operation is obtained.

Holt teaches that it is well known to provide a bias circuit and power supply circuit so that the amplifier can operate, i.e. amplify and to choose the bias level, so that a non-linear operation is obtained. Note that if a bipolar is used the power supply would be to the collector. Nonlinear operation results in the more efficient use of a amplifier for the transistor is not on all the time, Thus, the selection of the class of operation is merely the selection of a result effective variable that determines the energy consumption of the amplifier.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Taniguchi with a bias control circuit(s)/power supply circuits (level control circuits) that biases and supplies power to the first and second amplifiers such that non-linear operation is obtained for these amplifiers because, as the reference is silent on the exact biasing/power supply circuit one of ordinary skill in the art would have been motivated to use any conventional art recognized equivalent biasing circuit and power supply circuit therewith such as non-linear biasing/power supply arrangements of Holt. In addition, one of ordinary skill would have been motivated to do so because providing a bias circuit to cause operation in the non-linear region has the added advantage of providing the most energy efficient amplification of the input signal as taught by Holt.

With respect to claims like claims 11 and 12 the delay circuits of Taniguchi are quarter wavelength lines. It is well known in the art that a delay line can be composed of an inductor and one or more capacitors. These are art-recognized equivalents. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the inductor with one or more capacitors for the transmission delay lines of Taniguchi since the examiner takes Official Notice of the equivalence of the inductor with at one or more capacitors and the transmission delay line for use in the circuitry art and the selection of any of these known equivalents to provide delay/impedance inversion would be within the level of ordinary skill in the art.

As it relates to claims like claims 13 and 18, bipolar/heterojunction elements are well known to be art recognized equivalents to that of FETs. Thus it would have been obvious to one of ordinary skill in

the art at the time the invention was made to have substituted bipolar transistors for the FET transistors of Taniguchi since the examiner takes Official Notice of the equivalence of the bipolar/heterojunction element and FET element for use in the circuitry art and the selection of any of these known equivalents to provide amplification would be within the level of ordinary skill in the art. Note that the step/structure of applying a first output level control signal to a collector of the first amplifier "subsection" would be an obvious consequence of the combination made obvious above.

Claims 2, 4, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. 5,162,756 (Taniguchi) in view of Holt as applied to claims 1, 6, and 11-16 above, and further in view of Cheng et al. 2002/0190790 (Cheng).

All the reasoning as applied in the rejection of claims 1, 6, and 11-16 and the following: Taniguchi fails to describe using the biasing arrangement to disable one or more of the amplifiers in accordance with the power level one wants to obtain.

Cheng teaches that one can selectively supply the bias voltages each of the parallel-connected amplifiers so as to control the operation of these amplifiers, i.e. whether they are on or off. This controls the amount of power delivered to the load (See page "4" paragraph numbered "[0037]".),

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the bias control circuit of Taniguchi in view of Holt selectively control the bias voltages to the respective amplifiers of the arrangement. One of ordinary skill would have been motivated to do so as to control the amount of output power as taught by Cheng.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi, Holt and Cheng as applied to claims 2, 4, 17 and 20 above, and further in view of Atwater 4,189,732 (Atwater).

Taniguchi, Holt and Cheng fail to disclose the power supply arrangement as claimed. Holt is silent on the exact power supply circuit.

The only Figure of Atwater discloses a well-known circuit for providing a power supply voltage to an amplifier. This circuit includes a transistor 12, and an inductor 33 connected in series between the power supply voltage at 10 and the amplifier 46. This provides the "right" power supply level to the amplifier without supplying excess power to the amplifier that would have to be dissipated by the amplifier (See column 4, around line 44.).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have employed the circuit like Atwater for each of the amplifier circuits in the

combination of Taniguchi, Cheng and Holt because, as these references are silent on the exact power supply circuit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent power supply circuit for the amplifiers such as the conventional power supply circuit shown by Atwater. Additionally, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a power supply circuit like that of Atwater for each amplifier in the combination of Taniguchi, Cheng and Holt for one of ordinary skill in the art would have been motivated to do so as to provide a correct amount of power while preventing excess power to the amplifiers as taught by Atwater.

Note that just like in applicant's disclosed invention the term ramp is to signify the ramping of the voltage when the supply voltage is supplied to the amplifier. This is caused by the inductor and thus when the power is first applied to the power supply 11 of Atwater the voltage applied to the amplifier is in the form of a ramp. Therefore it is an obvious consequence of the combination made obvious above that the first and second output level control signals are ramp signals as meant by applicant. Also note that the claimed specific inductor/transistor combinations are an obvious consequence of the above combination.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi and Holt as applied to claims 1,6, and 11-16 above, and further in view of Sevic et al. 6,069,525 (Sevic).

Taniguchi and Holt both fail to disclose the controlling of both the bias and the power supply voltage in response to an analog level control signal.

Figure 1 of Sevic et al. clearly discloses a control circuit arrangement that controls both the bias voltage and the power supply voltage in response to an analog level control signal "MODE SELECT". This enables the efficiency of the amplifier arrangement that contains a plurality of parallel-connected amplifiers to be varied.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the bias/level control arrangement of Taniguchi to control both the bias voltage and the power supply voltage in response to an analog level control signal. One of ordinary skill would have been motivated to provide such an arrangement so as to vary the efficiency of amplification as taught by Sevic.

Claims 5, 7-10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi and Holt as applied to claims 1, 6, and 11-16 above, and further in view of Atwater 4,189,732 (Atwater).

Taniguchi fails to disclose the power supply arrangement as claimed. Holt is silent on the exact power supply circuit.

The only Figure of Atwater discloses a well-known circuit for providing a power supply voltage to an amplifier. This circuit includes a transistor 12, and an inductor 33 connected in series between the power supply voltage at 10 and the amplifier 46. This provides the "right" power supply level to the amplifier without supplying excess power to the amplifier that would have to be dissipated by the amplifier (See column 4, around line 44.).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have employed the circuit like Atwater for each of the amplifier circuits in the combination of Taniguchi and Holt because, as these references are silent on the exact power supply circuit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent power supply circuit for the amplifiers such as the conventional power supply circuit shown by Atwater. Additionally, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a power supply circuit like that of Atwater for each amplifier in the combination of Taniguchi and Holt for one of ordinary skill in the art would have been motivated to do so as to provide a correct amount of power while preventing excess power to the amplifiers as taught by Atwater.

Note that just like in applicant's disclosed invention the term ramp is to signify the ramping of the voltage when the supply voltage is supplied to the amplifier. This is caused by the inductor and thus when the power is first applied to the power supply 11 of Atwater the voltage applied to the amplifier is in the form of a ramp. Therefore it is an obvious consequence of the combination made obvious above that the first and second output level control signals are ramp signals as meant by applicant. Also note that the claimed specific inductor/transistor combinations are an obvious consequence of the above combination.

Response to Arguments

Applicant's arguments filed 08-12-2005 have been fully considered but they are not persuasive.

Applicant's assumes that the examiner's interpretation is that "Taniguchi includes a first amplifier FET_1 that is configured to receive an input signal that is the unmarked signal at the node that directly connects elements L_1, L_3, and L_4. Note that the first amplifier receives this signal through element L_3.". The examiner's position is and has been that arguments are that "Taniguchi includes a first amplifier "subsection" FET_1 (Herein and throughout referred to just as the first amplifier.) that is configured to receive an input signal that is the unmarked signal at the node that directly connects elements L_1, L_3, and L_4. Note that the first amplifier receives this signal through element L_3.". The claim language does not exclude elements between the input signal and the

first amplifier that receives this signal as the examiner clearly points out. It appears that applicant is implying in the arguments that there cannot be any delay element in between the input signal and the first amplifier but this would not be giving the broadest reasonable interpretation to the claimed invention (See MPEP 2111). Thus applicant's arguments are not persuasive.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
August 21, 2005

Michael B Shingleton
Primary Examiner
Group Art Unit 2817